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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,934	03/06/2002	Amir Alon	IL920020007US1	7058

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IBM CORPORATION
INTELLECTUAL PROPERTY LAW DEPT.
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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,934	ALON ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2- 9, 11-18, 23-24 and 26-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2- 9, 11-18, 23-24 and 26-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 23, 24 and 26-29 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form.

2. Claims 6, 15 and 17 are objected to:

the recitation of "AMS" is not clear to what applicants intend to mean. Additional information should be provided.

3. Claim 9 is objected to:

the recitation of "TEM impedance" is not clear to what applicants intend to mean. Additional information should be provided.

4. Claim 32 is objected to:

the recitation of "critical interconnect lines" and "transmission line" are not clear to what applicants intend to mean. Additional information should be provided.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 2- 9, 11-18, 23-24 and 26-35 are rejected under 35 U.S.C. 102(b) as being unpatentable by Luk et al. (US Patent 5,883,814).

As to claims 2, 6, 15, 17, 30, 31, 32, 34 and 35 Luk discloses system-on-chip layout compilation including:

(2) An integrated circuit design kit/system comprising:

means (tools/simulators/synthesizers) for generating one or more circuit component topologies (layout) (col.5, ll.56-67; col.6, ll.1-11; col.7, ll.4-22; col.8, ll.14-17; col.10, ll.58-67; col.11, ll.1-5); and

means (tools/simulators/synthesizers) for designing one or more transmission line (interconnects/wires/critical signal nets/critical paths) topologies (layout), for analog and mixed signal (AMS) circuit (digital and analog subsystems in one circuit) design (col.3, ll.52-58; col.5, ll.56-67; col.6, ll.1-11; col.8, ll.39-53 and ll.66-67; col.9, ll.1-31; col.15, ll.1-9; col.16, ll.1-3);

(6) A design topology (layout) of AMS transmission lines (interconnects/wires/critical signal nets/critical paths) (col.3, ll.52-58; col.5, ll.56-67; col.6, ll.1-11; col.8, ll.39-53 and ll.66-67; col.9, ll.1-31; col.15, ll.1-9; col.16, ll.1-3);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of transmission lines (col.3, ll.52-58; col.5, ll.56-67; col.6, ll.1-11 and ll.18-24; col.7, ll.4-22; col.8, ll.14-17; col.8, ll.39-53 and ll.66-67; col.9, ll.1-31; col.10, ll.58-67; col.11, ll.1-5; col.15, ll.1-9; col.16, ll.1-3);

(17) A computer software circuit design product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy (generating a coded output data stream) said circuit design product, said circuit design product comprising means for designing topology of transmission lines (col.3, ll.52-58; col.5, ll.56-67; col.6, ll.1-11; col.7, ll.4-22; col.8, ll.14-17; col.8, ll.39-53 and ll.66-67; col.9, ll.1-31; col.10, ll.58-67; col.11, ll.1-5; col.15, ll.1-9; col.16, ll.1-3);

(30) A method for designing integrated circuits wherein defining a chip architecture and a floor plan comprises defining critical interconnect wires (col.5, ll.56-67; col.6, ll.1-11; col.9, ll.15-31);

(31) a system for integrated circuit design comprising:

means (tools/simulators/synthesizers) for designing a high level circuit design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks (macros) and their locations are defined, and further including one or more transmission line (interconnects/wires/critical signal nets/critical paths) topologies (layout) (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.15, ll.1-9; col.16, ll.1-3);

means (tools/simulators/synthesizers) for designing a schematic design at least including one or more circuit components and one or more transmission lines models (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.15, ll.1-9; col.16, ll.1-3); and

means/tools for designing a physical layout at least including said one or more

circuit components and said one or more transmission line topologies (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.15, ll.1-9; col.16, ll.1-3);

(32) A method for designing integrated circuits (IC), said method comprising steps of:

a) defining a chip architecture and floor plan (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.15, ll.1-9; col.16, ll.1-3);

b) identifying one or more critical interconnect lines/wire and defining one or more transmission line topologies for said critical interconnect lines (col.5, ll.56-67; col.6, ll.1-11; col.9, ll.15-31);

c) determining a schematic design (logic gate level circuit description) of said IC from said chip architecture, floor plan and said transmission line topologies (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.15, ll.1-9; col.16, ll.1-3); and

d) defining a physical layout of said IC at least from said chip architecture, floor plan and said line topologies (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.15, ll.1-9; col.16, ll.1-3);

(34) A system for integrated circuit design comprising:

means/tools for designing a schematic design at least including one or more circuit components and one or more transmission lines models, wherein said one or more transmission lines are models parameterized cells of one or more transmission lines topologies (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-

32; col.10, ll.12-37; col.15, ll.1-9; col.16, ll.1-3);

(35) A method for designing integrated circuits (IC), said method comprising:

means (tools/simulators/synthesizers) for designing a schematic design (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.10, ll.12-37; col.15, ll.1-9; col.16, ll.1-3); and

means (tools/simulators/synthesizers) for designing a physical layout including at least one or more circuit components and one or more transmission line topologies, wherein said one or more transmission line topologies are parameterized cells of transmission lines (col.3, ll.52-58; col.5, ll.55-63; col.8, ll.39-53 and ll.66-67; col.9, ll.1-32; col.10, ll.12-37; col.15, ll.1-9; col.16, ll.1-3).

As to claims 3-5, 7-9, 11-14, 16, 18, 23, 24, 26-29 and 33 Luk recites:

(3), (7) The kit wherein said transmission line topologies are predefined (col.10, ll.58-67; col.11, ll.1-5);

(4) The kit of claim 2 further comprising one or more circuit component models (col. 11, ll.6-28);

(5) The kit of claim 2 and further comprising one or more transmission line models (col.3, ll.52-58; col.5, ll.56-67; col.6, ll.1-11; col.8, ll.39-53 and ll.66-67; col.9, ll.1-31; col.15, ll.1-9; col.16, ll.1-3);

(8) The topology of claim 6 comprising a definite current return path (col.4, ll.47-67);

(9), (26), (27) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters (col.2, ll.1-13; col.7, ll.58-67; col.8, ll.1-13; col.10, ll.58-67; col.11, ll.1-5);

(11)-(14) The design topology wherein said topology comprises one or more signal wires and one or more shielding wires (col.8, ll.39-53; col.10, ll.58-67; col.11, ll.1-5);

(16), (18) The product further comprising instructions, cause said computer lo create a design model of transmission lines (col.5, ll.56-63; col.6, ll.18-24).

(23), (29), (33) The method, wherein the step of designing comprises choosing from a set of predefined parameterized design topologies/cells ([0033]; [0034]);

(28) The method according to claim 32. wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, timing requirements (col.7, ll.58-67; col.8; ll.1-13; col.9, ll.15-31).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 2- 9, 11-18, 23-24 and 26-35 are rejected under 35 U.S.C. 102(e) as being unpatentable by Saito (Pub. No.: US 2002/0095648).

As to claims 2, 6, 15, 17, 30, 31, 32, 34 and 35 Saito discloses Layout method of analog/digital mixed semiconductor integrated circuit including:

(2) An integrated circuit design kit/system comprising:

means (tools/simulators/synthesizers) for generating one or more circuit component topologies (layout) ([0032]-[0033]); and

means (tools/simulators/synthesizers) for designing one or more transmission line (interconnects/wires/critical signal nets/critical paths) topologies (layout), for analog and mixed signal (AMS) circuit (digital and analog subsystems in one circuit) design ([0037]);

(6) A design topology (layout) of AMS transmission lines (interconnects/wires/critical signal nets/critical paths) ([0037]);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of transmission lines ([0032]-[0033]; [0037]);

(17) A computer software circuit design product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy said circuit design product, said circuit design product comprising means for designing topology of transmission lines ([0032]-[0033]; [0037]);

(30) A method for designing integrated circuits wherein defining a chip architecture and a floor plan comprises defining critical interconnect wires ([0032]-[0034]; [0037]);

(31) a system for integrated circuit design comprising:

means (tools/simulators/synthesizers) for designing a high level circuit design, said high level circuit design including a chip architecture and a floor plan, whereby major design blocks (macros) and their locations are defined, and further including one or more transmission line (interconnects/wires/critical signal nets/critical paths) topologies (layout) ([0032]-[0034]; [0037]);

means (tools/simulators/synthesizers) for designing a schematic design at least including one or more circuit components and one or more transmission lines models ([0032]-[0034]; [0037]); and

means/tools for designing a physical layout at least including said one or more circuit components and said one or more transmission line topologies ([0032]-[0034]; [0037]);

(32) A method for designing integrated circuits (IC), said method comprising steps of:

a) defining a chip architecture and floor plan ([0032]-[0034]; [0037]);

b) identifying one or more critical interconnect lines/wire and defining one or more transmission line topologies for said critical interconnect lines ([0032]-[0034]; [0037]);

c) determining a schematic design (logic gate level circuit description) of said IC

from said chip architecture, floor plan and said transmission line topologies ([0032]-[0034]; [0037]); and

d) defining a physical layout of said IC at least from said chip architecture, floor plan and said line topologies ([0032]-[0034]; [0037]);

(34) A system for integrated circuit design comprising:

means/tools for designing a schematic design at least including one or more circuit components and one or more transmission lines models, wherein said one or more transmission lines are models parameterized cells of one or more transmission lines topologies ([0032]-[0034]; [0037]; [0041]- [0042]);

(35) A method for designing integrated circuits (IC), said method comprising:

means (tools/simulators/synthesizers) for designing a schematic design ([0032]-[0034]; [0037]); and

means (tools/simulators/synthesizers) for designing a physical layout including at least one or more circuit components and one or more transmission line topologies, wherein said one or more transmission line topologies are parameterized cells of transmission lines ([0032]-[0034]; [0037]).

As to claims 3-5, 7-9, 11-14, 16, 18, 23, 24, 26-29 and 33 Luk recites:

(3), (7) The kit wherein said transmission line topologies are predefined ([0036]);

(4) The kit of claim 2 further comprising one or more circuit component models ([0036]);

(5) The kit of claim 2 and further comprising one or more transmission line models ([0036];[0037]);

(8) The topology of claim 6 comprising a definite current return path ([0005]-[0006]);

(9), (26), (27) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters ([0032]-[0033]; [0037]);

(11)-(14) The design topology wherein said topology comprises one or more signal wires and one or more shielding wires ([0008]; [0035]);

(16), (18) The product further comprising instructions, cause said computer lo create a design model of transmission lines ([0032]-[0033]; [0037]);

(23), (29), (33) The method, wherein the step of designing comprises choosing from a set of predefined parameterized design topologies/cells ([0032]-[0033]; [0037]; [0041]-[0042]);

(28) The method according to claim 32, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment, timing requirements ([0041]-[0042]).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 2-7, 9 and 15-18 are rejected under 35 U.S.C. 102(b) as being unpatentable by Chao et al. (US Patent 5,031,111).

Chao discloses automated technique for the design of microwave and similar circuits using computer system including:

As to claims 2, 6, 15 and 17 Chao describes:

(2) An integrated circuit design kit/system comprising (col.4, ll.40-67; col.5, ll.1-10; col.9, ll.34-59):

means/tools for generating one or more circuit component topologies (col.1, ll.5-10; col.2, ll.24-54; col.4, ll.15-39); and

means/tools for designing one or more transmission line topologies, for analog and mixed signal (AMS) circuit (microwave and similar circuit) design (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54);

(6) A design topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54);

(15) A computer software product for designing an AMS integrated circuit (microwave and similar circuit), said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to create a design topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54; col.9, ll.60-67; col.10, ll.1-8);

(17) A computer software circuit design product for designing an AMS integrated circuit (microwave and similar circuit), said product comprising a computer readable medium in which program instructions are stored, which when read by a computer, cause said computer to deploy (generating a coded output data stream) said circuit design product, said circuit design product comprising means for designing topology of transmission lines (col.4, ll.15-40; col.5, ll.41-65; col.7, ll.42-54; col.9, ll.60-67; col.10, ll.1-8 and ll.26-54);

As to claims 3-5, 7, 9, 16 and 18 Chao recites:

(3) The kit of claim 2 wherein said transmission line topologies are predefined (in a library) (col.5, ll.11-40);

(4) The kit of claim 2 further comprising one or more circuit component models (col.2, ll.24-67; col.3, ll.1-40);

(5) The kit of claim 2 and further comprising one or more transmission line models (col.2, ll.24-67; col.3, ll.1-40);

(7) The design topology of claim 6 wherein said topology is predefined (col.5, ll.11-40);

(9) The design topology of claim 6 wherein said design topology comprises a model describing one or more of electrical parameters (col.4, ll.15-39);

(16), (18) The product further comprising instructions, which when read by a computer, cause said computer lo create a design model of transmission lines (col.2, ll.24-67; col.3, ll.1-40).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claim 6 is rejected under 35 U.S.C. 102(e) as being unpatentable by Pileggi et al. (US Patent 6,286,128).

As to claim 6 Pileggi discloses method for design optimization using logical and physical information including:

A design topology (net topology) of AMS transmission lines (mixed mode signals on RF transmission lines) (col.5, ll.62-67; col.6, ll.1-4; col.13, ll.46-58; col.14, ll.1-2).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 6, 15 and 17 is rejected under 35 U.S.C. 102(e) as being unpatentable by Boyle et al. (US Patent 6,557,145).

As to claim 6 Boyle recites:

(6) A design topology (net topology) of AMS transmission lines (mixed mode signals on RF transmission lines) (col.11, ll.53-58; col.19, ll.36-50);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a topology of transmission lines (col.3, ll.51-67; col.4, ll.1-4; col.11, ll.53-58; col.19, ll.36-50);

(17) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a design kit comprising a topology of critical interconnect lines (col.3, ll.51-67; col.4, ll.1-4; col.11, ll.53-58; col.19, ll.36-50).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 2-13, 15-18, 23-24, 26-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Dansky et al. (US Patent 6,342,823).

Dansky discloses system and method for reducing calculation complexity of lossy, frequency-dependent transmission-line computation including:

As to claims 2, 6, 15, 17, 30 and 32 Dansky recites:

(2) An integrated circuit design kit comprising:

means for generating or more circuit components topologies (col.5, ll.19-24); and

means for designing one or more transmission lines topologies for analog and mixed signal (AMS) circuit design(Abstract; col.5, ll.19-24);

(6) A design topology of AMS transmission lines (Abstract; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(15) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a topology of transmission lines (Abstract; col.2, ll.36-49; col.3, ll.26-48; col.5, ll.22-24; col.6, ll.64-67 and col.8, ll.1-5);

(17) A computer software product for designing an AMS integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a design kit comprising a topology of critical interconnect lines (Abstract; col.2, ll.36-49; col.3, ll.26-48; col.5, ll.19-24; col.6, ll.64-67 and col.8, ll.1-5);

(30) A method for designing integrated circuits wherein defining said chip architecture and a floor plan comprises defining critical interconnect wires (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67).

(32) A method for designing integrated circuit comprising:

(a) defining a chip architecture and a floor plan; (Abstract; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(b) identifying ore or more critical interconnect lines, and defining one or more transmission line topologies for said critical interconnect lines (Abstract; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(c) determining a schematic design of said IC from said chip architecture floor plan and said transmission line topologies (col.5, ll.22-24 and ll.34-35);

(d) defining a physical layout of said IC at least from said chip architecture floor plan and said transmission line topologies (col.5, ll.19-24).

As to claims 3-5, 7-9, 11-13, 23, and 27-28 Dansky discloses:

(3), (7), (23) The kit of, wherein said interconnect line topologies are predefined (col.5, ll.21-31);

(4) The kit of claim 2 and further comprising one or more circuit components models (col.5, ll.22-24 and ll.34-35);

(5) The kit of claim 2 and further comprising one or more critical interconnect lines models (col.5, ll.22-24 and ll.34-35);

(8) The topology of claim 6 comprising a definite current return path (col.3, ll.34-37 and col.4, ll.31-36);

(9), (27) The topology of claim 6 wherein said topology is supplemented by a model comprising one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters (col.2, ll.26-34 and col.3, ll.54-60);

(11) The topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires (col.2, ll.56-63);

(12) The topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires (col.3, ll.26-47);

(13) The topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire (col.3, ll.26-47);

(28) The method according to claim 19, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment and manual user selection (col.1, ll.17-19 and col.5, ll.21-31).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dansky.

With respect to claim 14 Dansky teaches the features above (for example col.2, ll.56-63 and col.3, ll.26-47) but lacks a system and method for IC design, where shielding wires may generate one or more shielding layers, witch is well known to a person of ordinary skills in the art at the time the invention was made.

It would have been obvious to a person of ordinary skills in the art at the time the

invention was made to employ Dansky's teaching regarding the method and system using shielding layers to improve shielding effect in case of need.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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VUTHE SIEK
PRIMARY EXAMINER